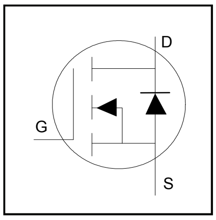
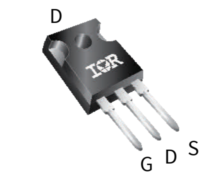
IR MOSFET - StrongIRFET™



V_{DSS}	250V
$R_{DS(on)}$ typ.	18mΩ
max	22mΩ
I_D	69A



TO-247AC
IRF250P225

Applications

- UPS and Inverter applications
- Half-bridge and full-bridge topologies
- Resonant mode power supplies
- DC/DC and AC/DC converters
- OR-ing and redundant power switches
- Brushed and BLDC Motor drive applications
- Battery powered circuits

G	D	S
Gate	Drain	Source

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Pb-Free ; RoHS Compliant ; Halogen-Free

Halogen-Free RoHS

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF250P225	TO-247AC	Tube	25	IRF250P225

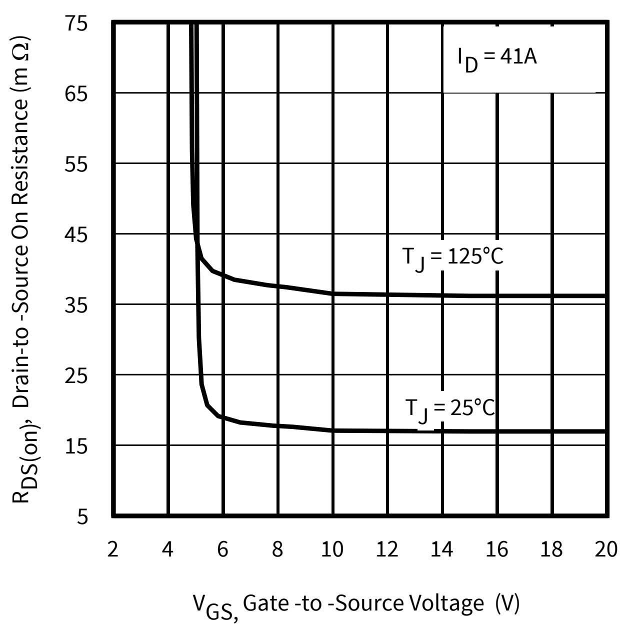


Figure 1 Typical On-Resistance vs. Gate Voltage

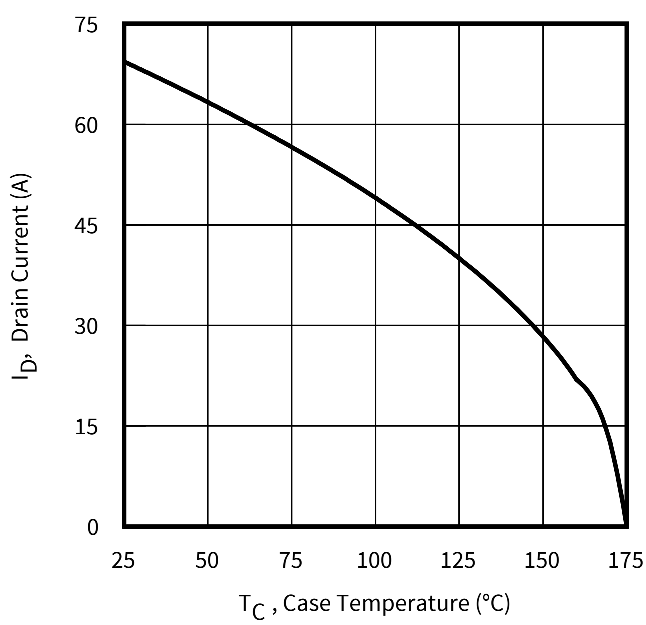


Figure 2 Maximum Drain Current vs. Case Temperature

Table of Contents

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1 Parameters 3
2 Maximum ratings, Thermal, and Avalanche characteristics 4
3 Electrical characteristics 5
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1 Parameters

Table1 Key performance parameters

Parameter	Values	Units
V_{DS}	250	V
$R_{DS(on)\ max}$	22	mΩ
I_D	69	A

2 Maximum ratings and thermal characteristics

Table 2 Maximum ratings (at T_J=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current	I_D	T_C = 25°C, V_{GS} @ 10V	69	A
Continuous Drain Current	I_D	T_C = 100°C, V_{GS} @ 10V	49	
Pulsed Drain Current ①	I_{DM}	T_C = 25°C	276	
Maximum Power Dissipation	P_D	T_C = 25°C	313	W
Linear Derating Factor		T_C = 25°C	2.1	W/°C
Gate-to-Source Voltage	V_{GS}	-	± 20	V
Operating Junction and Storage Temperature Range	T_J T_{STG}	-	-55 to + 175	°C
Soldering Temperature, for 10 seconds (1.6mm from case)	-	-	300	
Mounting Torque, 6-32 or M3 Screw	-	-	10 lbf·in (1.1 N·m)	-

Table 3 Thermal characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case ⑦	$R_{\theta JC}$	T_J approximately 90°C	-	-	0.48	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	-	-	0.24	-	
Junction-to-Ambient	$R_{\theta JA}$	-	-	-	40	

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ②	E_{AS} (Thermally limited)	444	mJ
Single Pulse Avalanche Energy ⑧	E_{AS} (Thermally limited)	489	
Avalanche Current ①	I_{AR}	See Fig 16, 17, 23a, 23b	A
Repetitive Avalanche Energy ①	E_{AR}		mJ

Notes:

① *Repetitive rating; pulse width limited by max. junction temperature.*
② *Limited by T_{Jmax}, starting T_J = 25°C, L = 0.52mH, R_G = 50Ω, I_{AS} = 41A, V_{GS} =10V.*
③ *$I_{SD} \leq 41A$, $di/dt \leq 926A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$.*
④ *Pulse width ≤400µs; duty cycle ≤2%.*
⑤ *C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
⑥ *C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
⑦ *R_θ is measured at T_J approximately 90°C.*
⑧ *Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 31A, V_{GS} =10V.*

3 Electrical characteristics

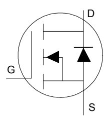
Table 5 Static characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 1mA	250	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D = 2.5mA ①	-	0.17	-	V/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 41A	-	18	22	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 270μA	2.0	-	4.0	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} =200V, V_{GS} =0V	-	-	1.0	μA
		V_{DS} =200V, V_{GS} = 0V, T_J =125°C	-	-	100	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate Resistance	R_G		-	2.7	-	Ω

Table 6 Dynamic characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit
Forward Trans conductance	gfs	V_{DS} = 50V, I_D =41A	72	-	-	S
Total Gate Charge	Q_g	I_D = 41A V_{DS} = 125V V_{GS} = 10V	-	64	96	nC
Gate-to-Source Charge	Q_{gs}		-	24	-	
Gate-to-Drain Charge	Q_{gd}		-	12	-	
Total Gate Charge Sync. (Qg– Qgd)	Q_{sync}		-	52	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 163V I_D = 41A R_G = 2.7Ω V_{GS} = 10V	-	17	-	ns
Rise Time	t_r		-	54	-	
Turn-Off Delay Time	$t_{d(off)}$		-	52	-	
Fall Time	t_f		-	36	-	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 50V f = 1.0MHz, See Fig.7	-	4897	-	pF
Output Capacitance	C_{oss}		-	505	-	
Reverse Transfer Capacitance	C_{rss}		-	6.1	-	
Effective Output Capacitance (Energy Related)	$C_{oss\ eff.(ER)}$	V_{GS} = 0V, V_{DS} = 0V to 200V ⑥	-	372	-	
Output Capacitance (Time Related)	$C_{oss\ eff.(TR)}$	V_{GS} = 0V, V_{DS} = 0V to 200V ⑤	-	607	-	

Table 7 Reverse Diode

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	69	A
Pulsed Source Current (Body Diode) ①	I_{SM}		-	-	276	
Diode Forward Voltage	V_{SD}	T_J = 25°C, I_S = 41A, V_{GS} = 0V ④	-	-	1.2	V
Peak Diode Recovery dv/dt ③	dv/dt	T_J = 175°C, I_S = 41A, V_{DS} = 250V	-	25	-	V/ns
Reverse Recovery Time	t_{rr}	T_J = 25°C; V_{DD} = 213V, I_F = 41A, di/dt = 100A/μs ④	-	113	-	ns
		T_J = 125°C	-	155	-	
Reverse Recovery Charge	Q_{rr}	T_J = 25°C	-	427	-	nC
		T_J = 125°C	-	878	-	
Reverse Recovery Current	I_{RRM}	T_J = 25°C	-	5.7	-	A

4 Electrical characteristic diagrams

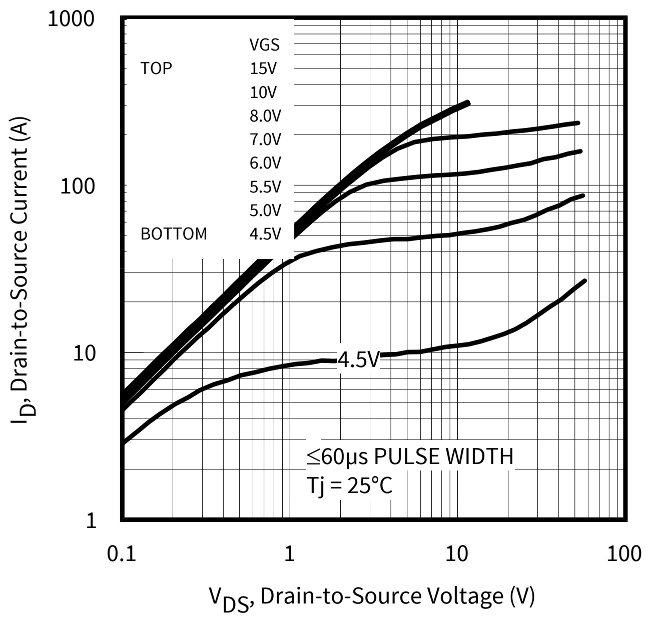


Figure 3 Typical Output Characteristics

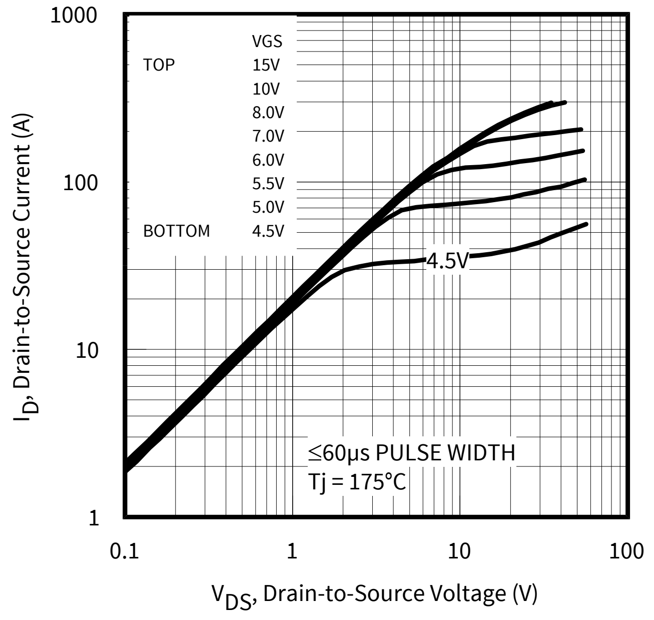


Figure 4 Typical Output Characteristics

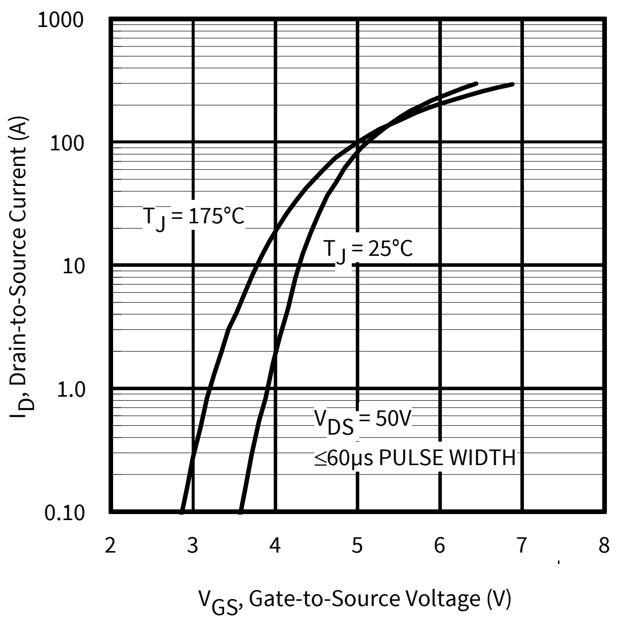


Figure 5 Typical Transfer Characteristics

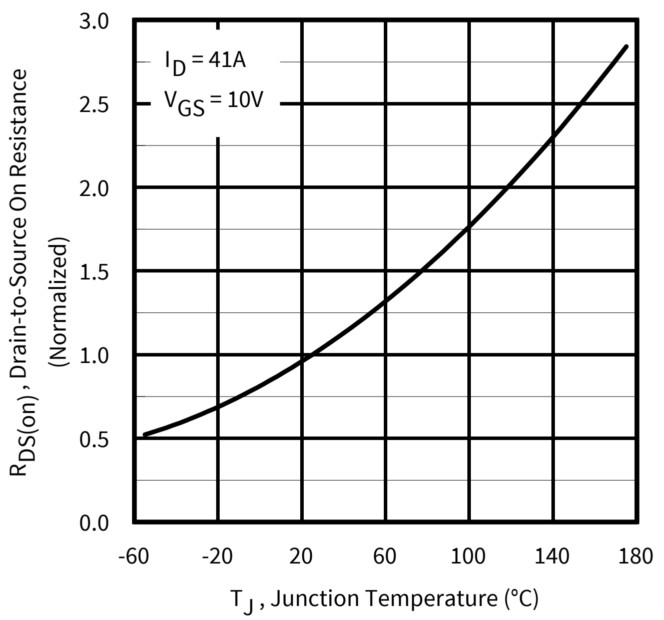


Figure 6 Normalized On-Resistance vs. Temperature

Electrical characteristic diagrams

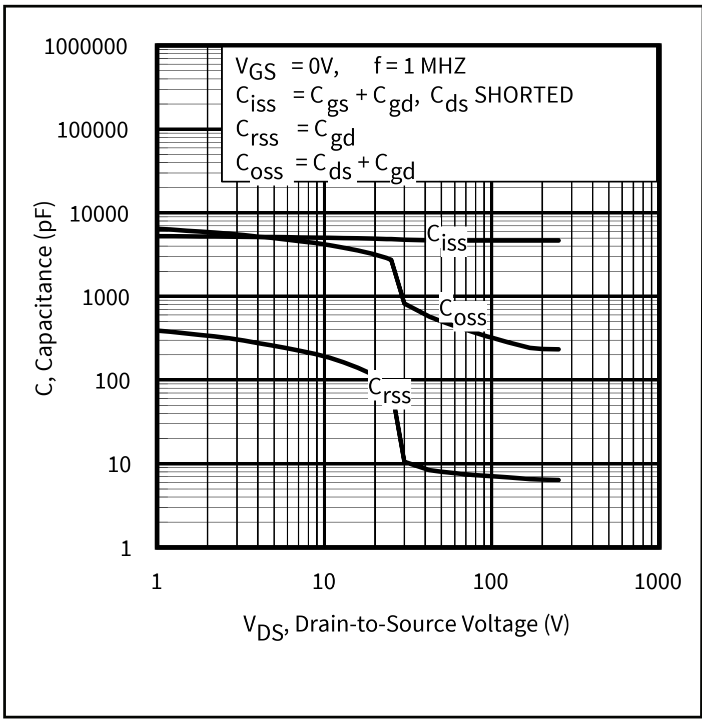


Figure 7 Typical Capacitance vs. Drain-to-Source Voltage

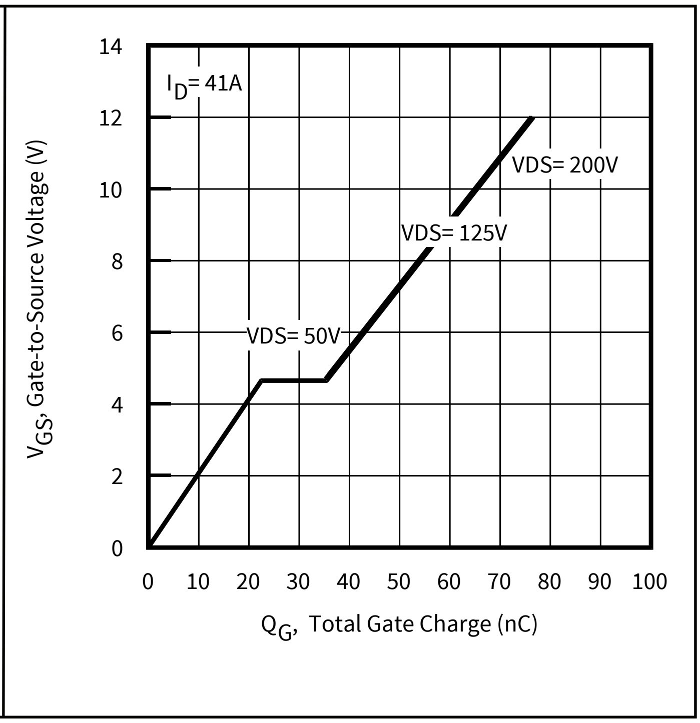


Figure 8 Typical Gate Charge vs. Gate-to-Source Voltage

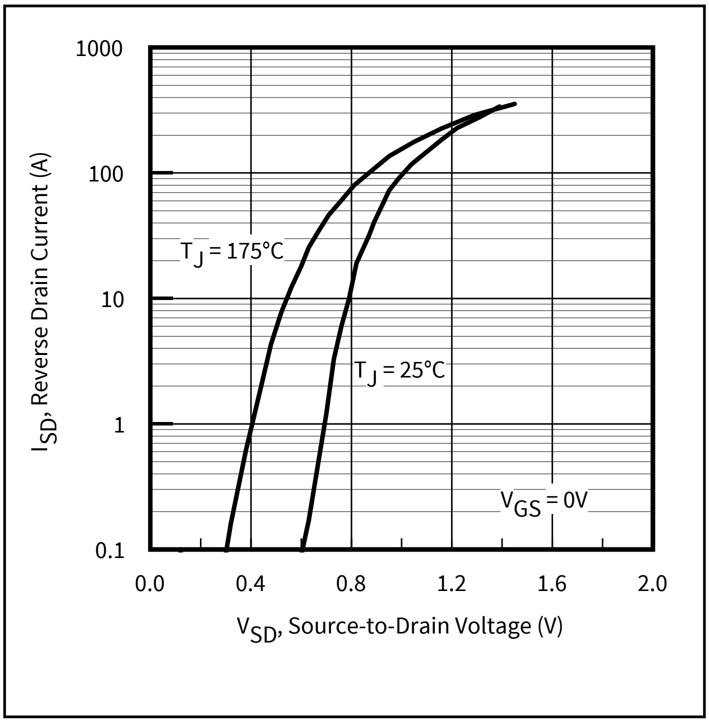


Figure 9 Typical Source-Drain Diode Forward Voltage

Electrical characteristic diagrams

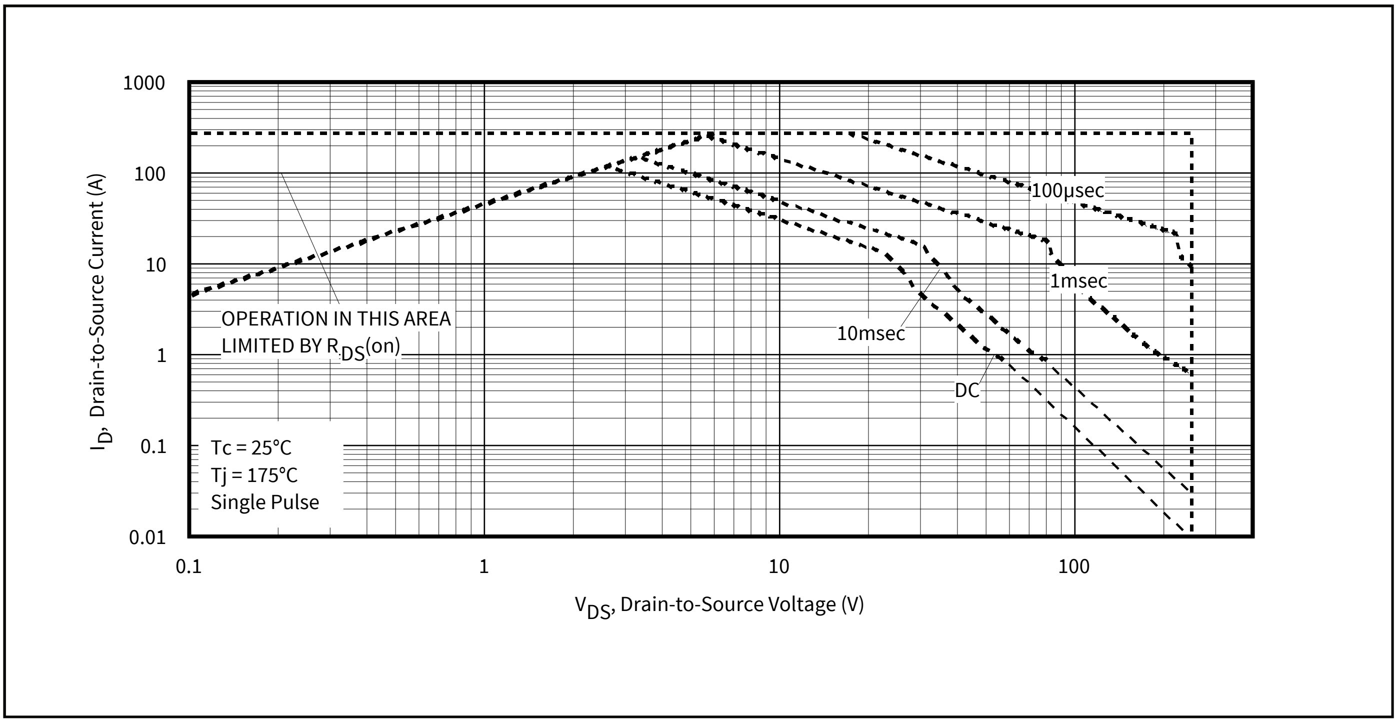


Figure 10 Maximum Safe Operating Area

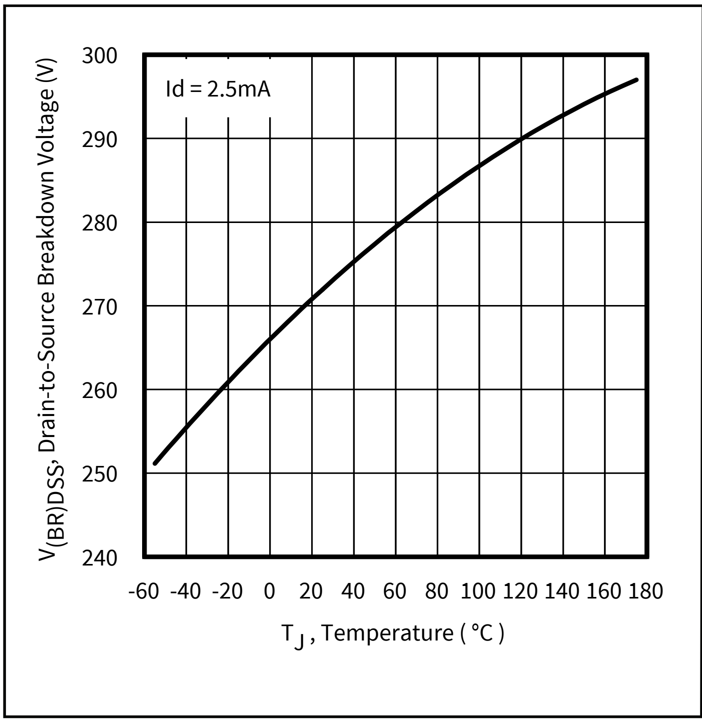


Figure 11 Drain-to-Source Breakdown Voltage

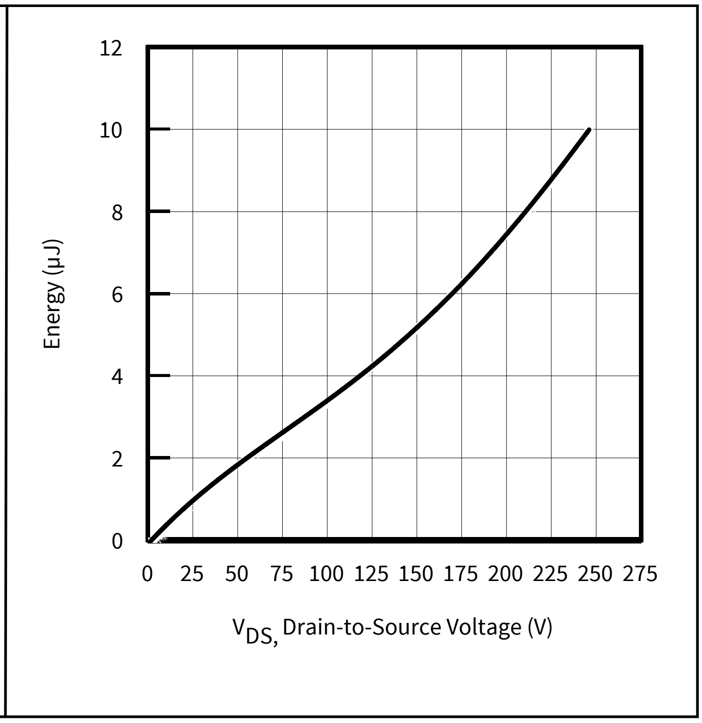
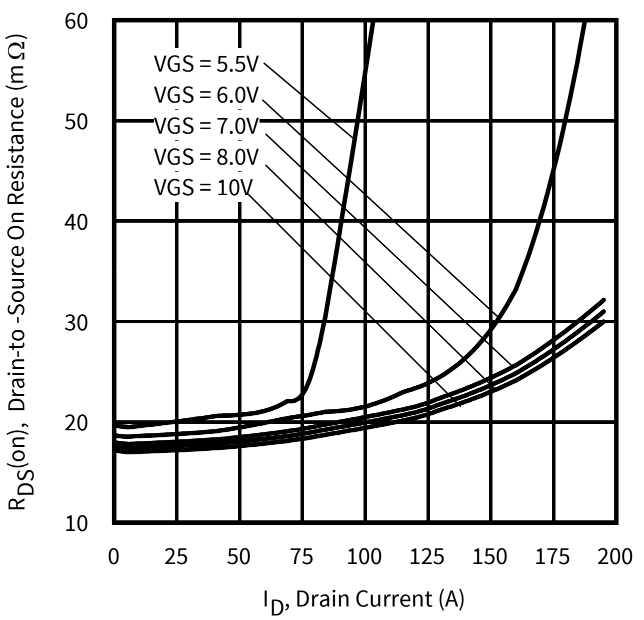


Figure 12 Typical Coss Stored Energy



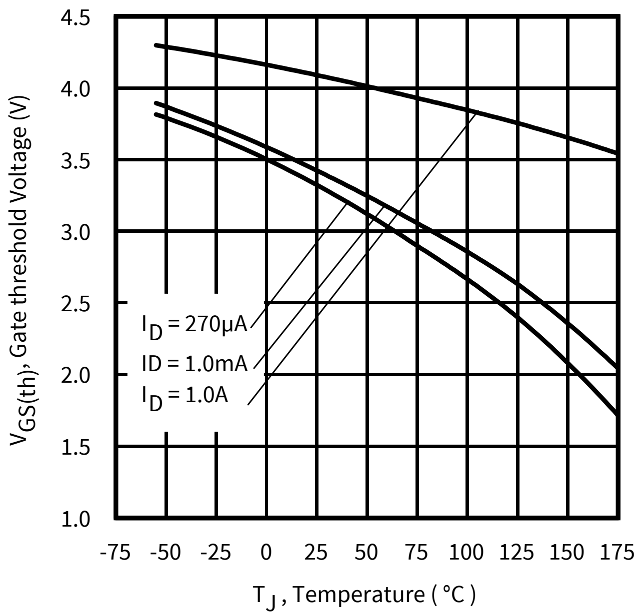


Figure 13 Typical On-Resistance vs. Drain Current

Figure 14 Threshold Voltage vs. Temperature

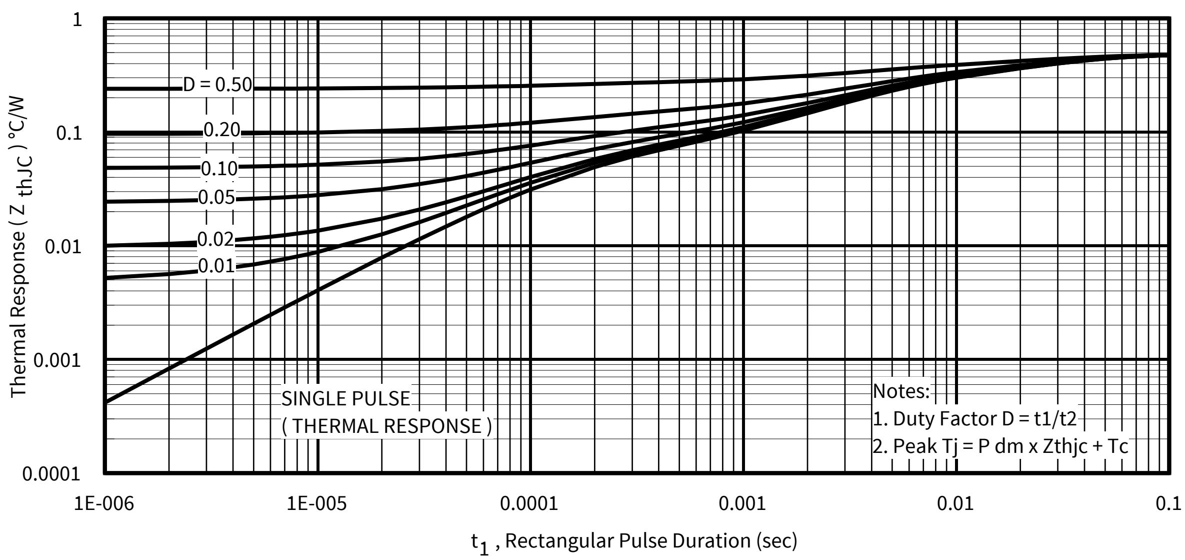


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

Electrical characteristic diagrams

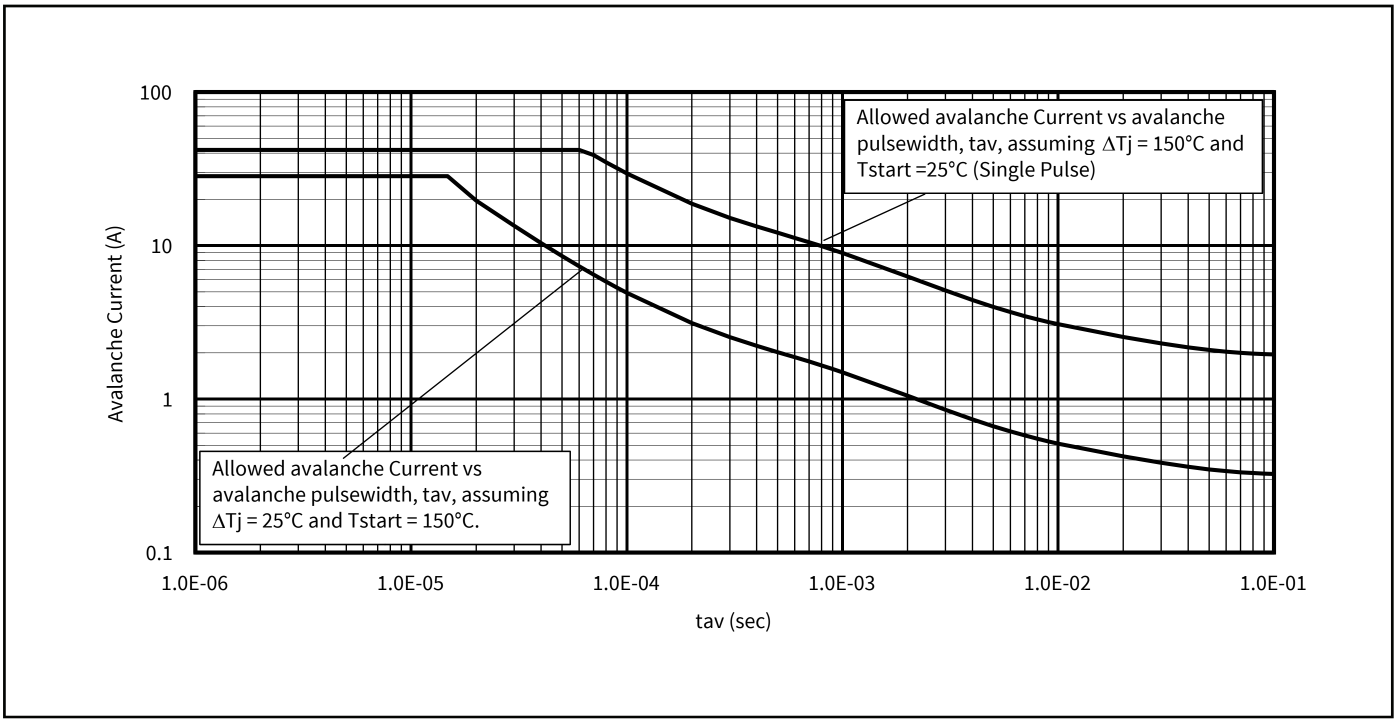


Figure 16 Avalanche Current vs. Pulse Width

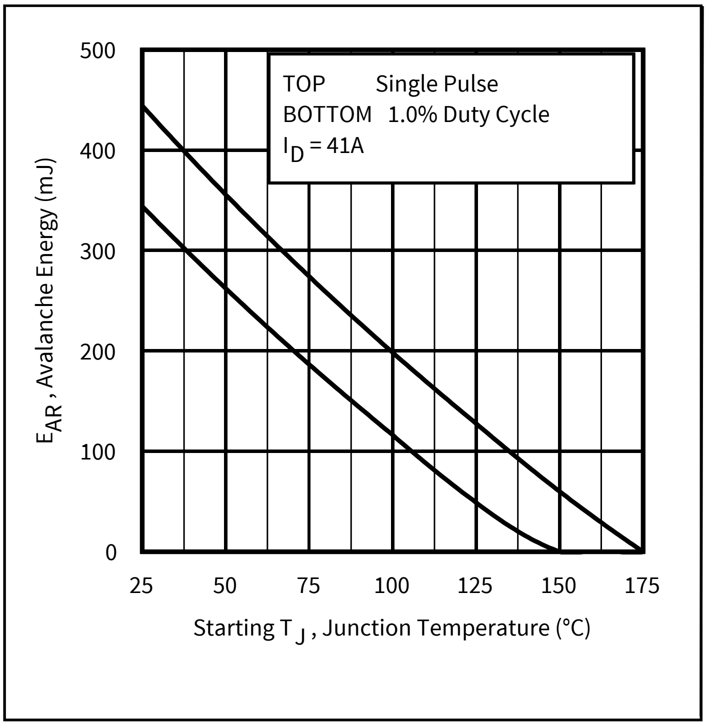
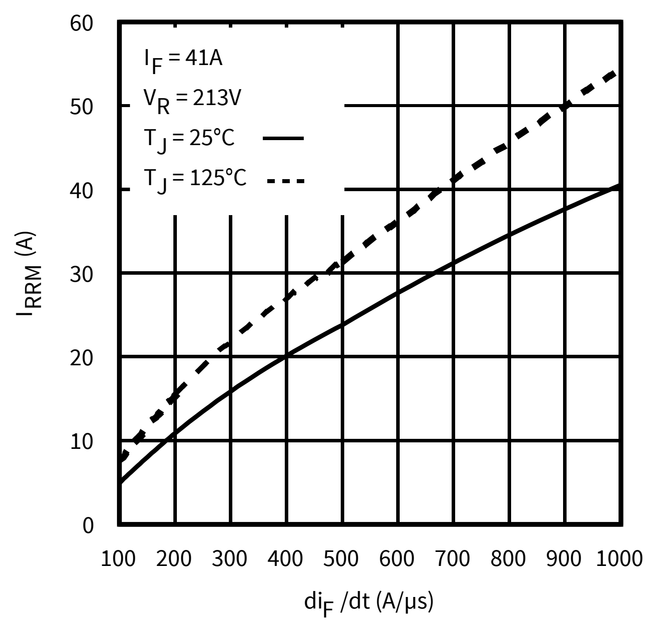


Figure 17 Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 16, 17:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. DT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$$PD\,(ave) = 1/2\,(1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$



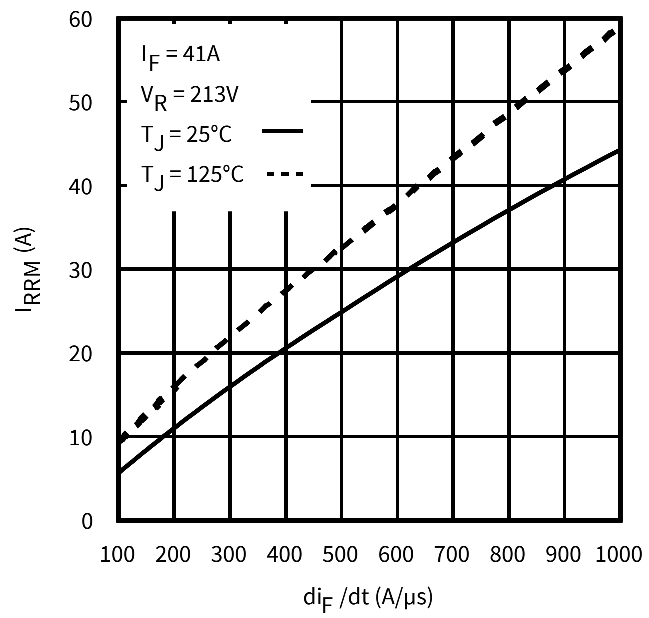
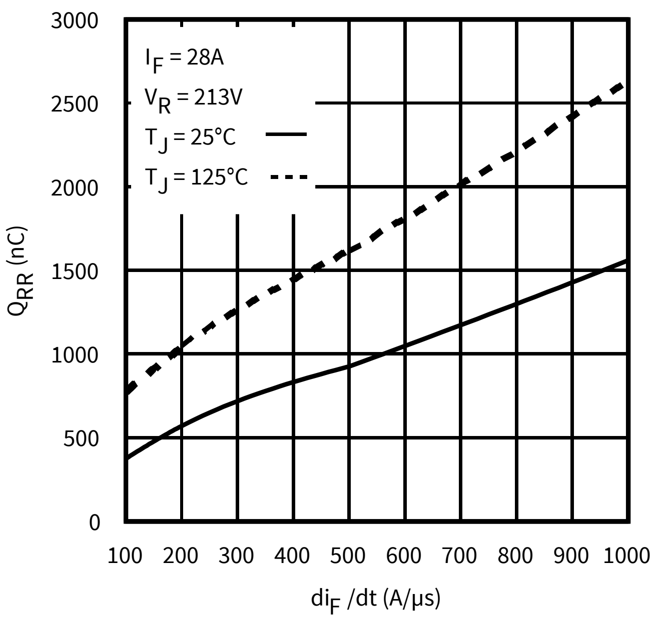


Figure 18 Typical Recovery Current vs. dif/dt

Figure 19 Typical Recovery Current vs. dif/dt



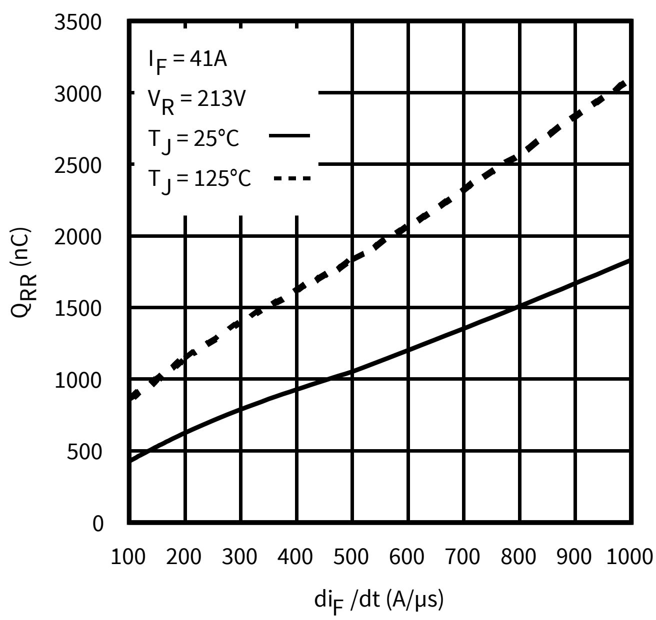


Figure 20 Typical Stored Charge vs. dif/dt

Figure 21 Typical Stored Charge vs. dif/dt

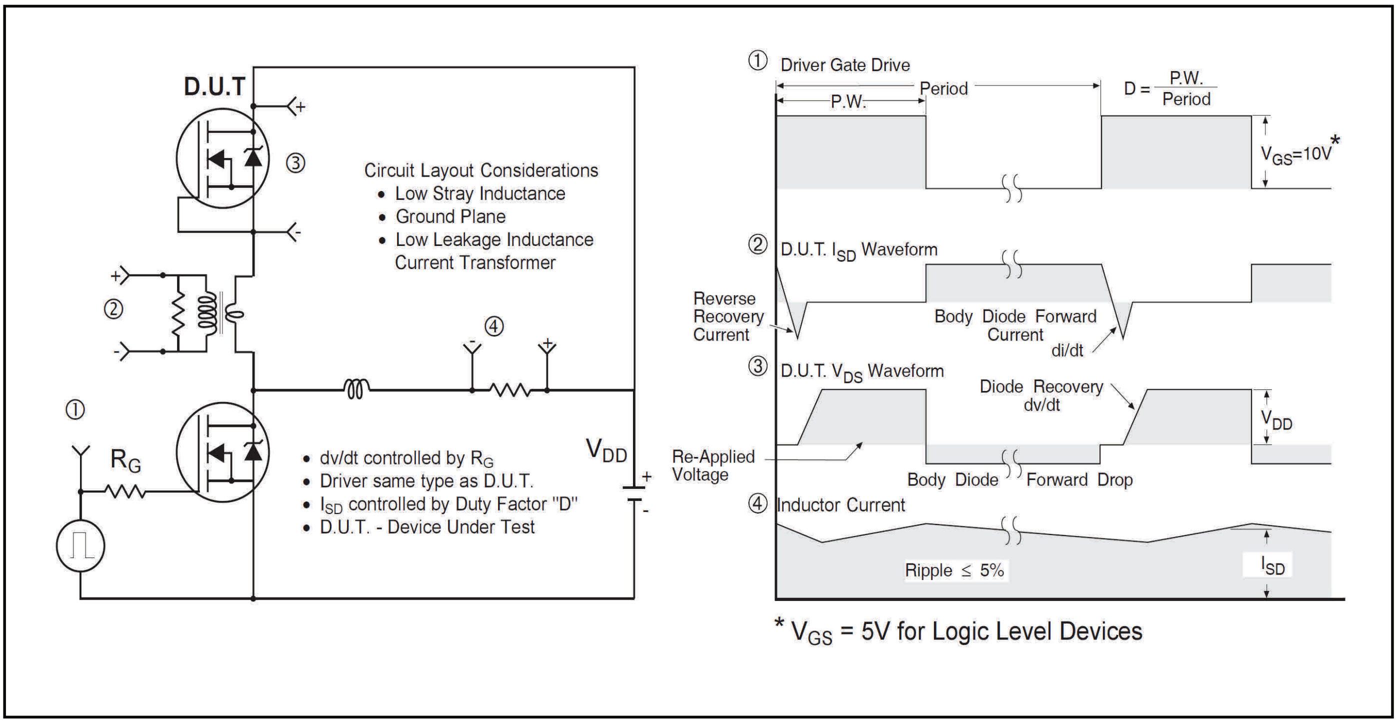


Figure 22 Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET™ Power MOSFETs

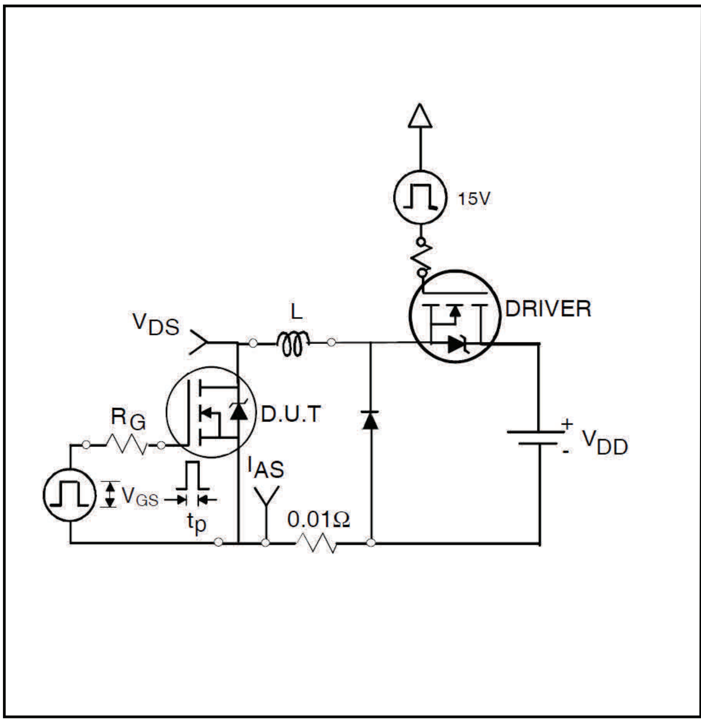


Figure 23a Unclamped Inductive Test Circuit

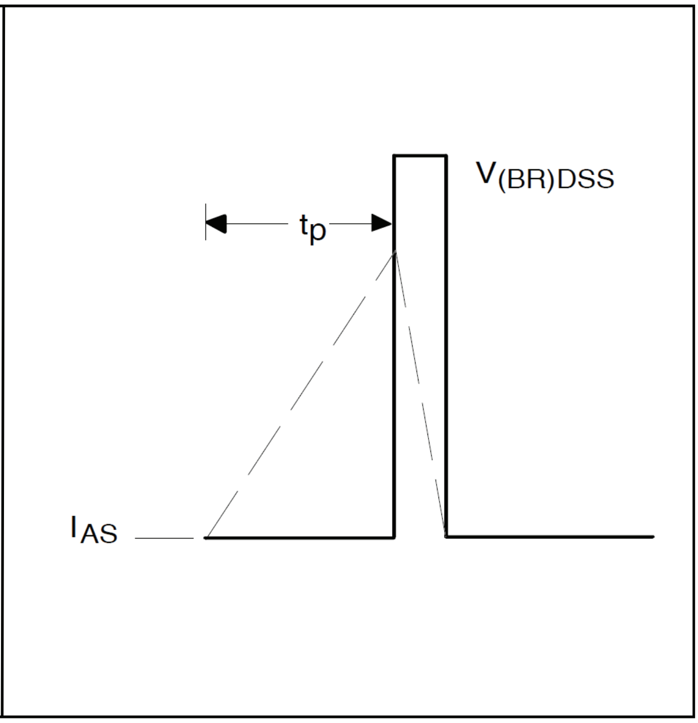


Figure 23b Unclamped Inductive Waveforms

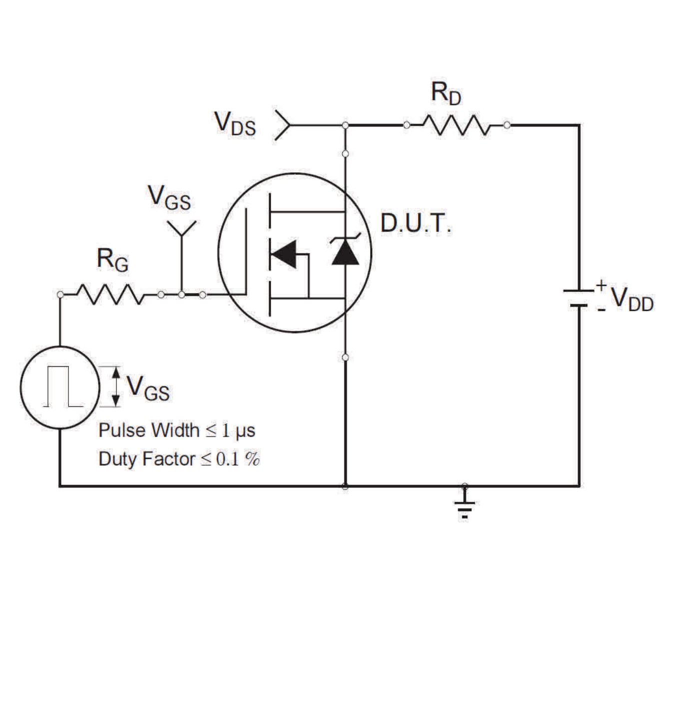


Figure 24a Switching Time Test Circuit

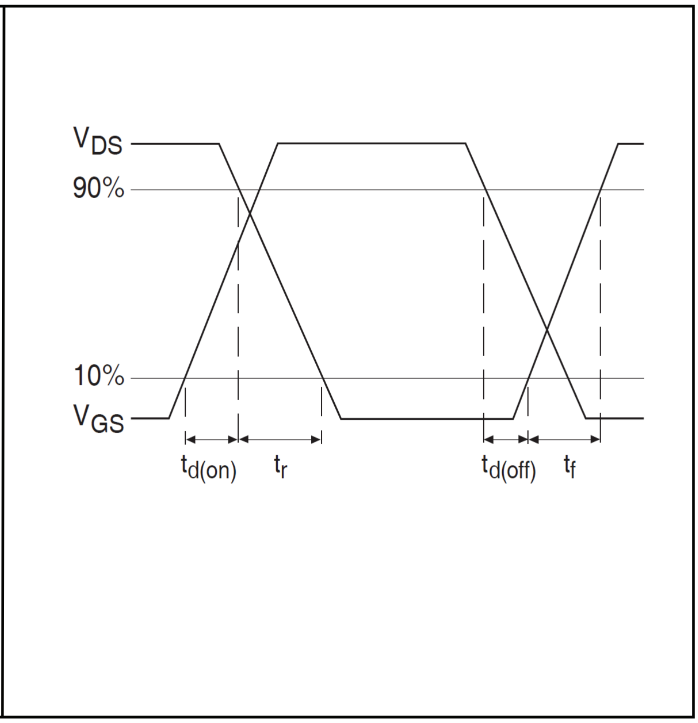


Figure 24b Switching Time Waveforms

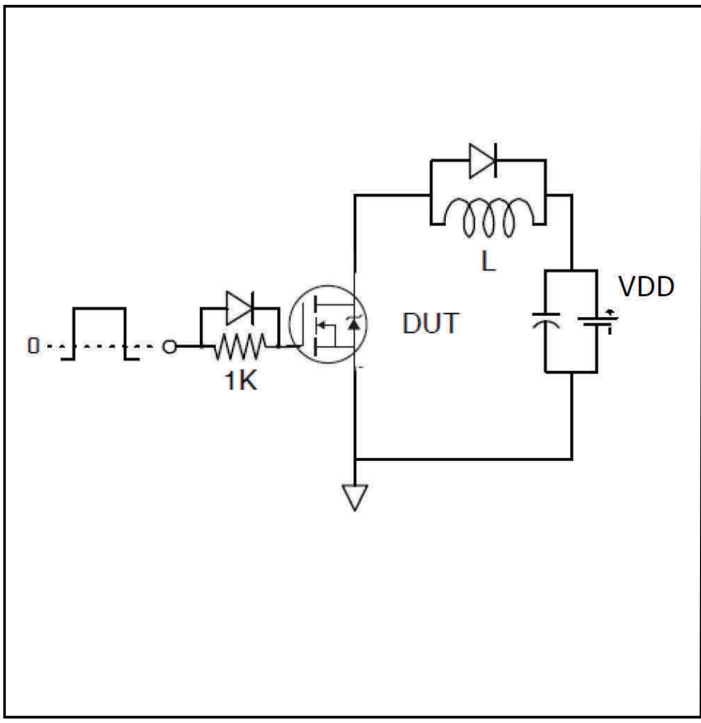


Figure 25a Gate Charge Test Circuit

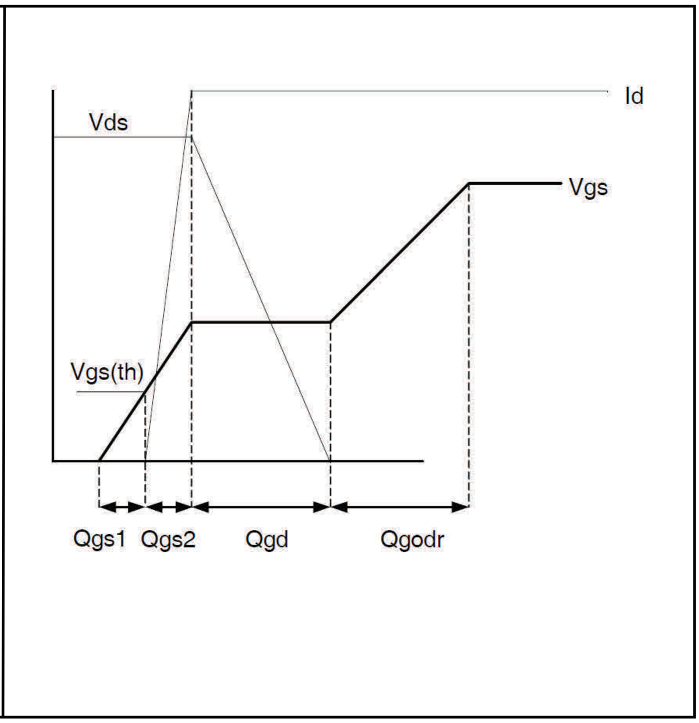
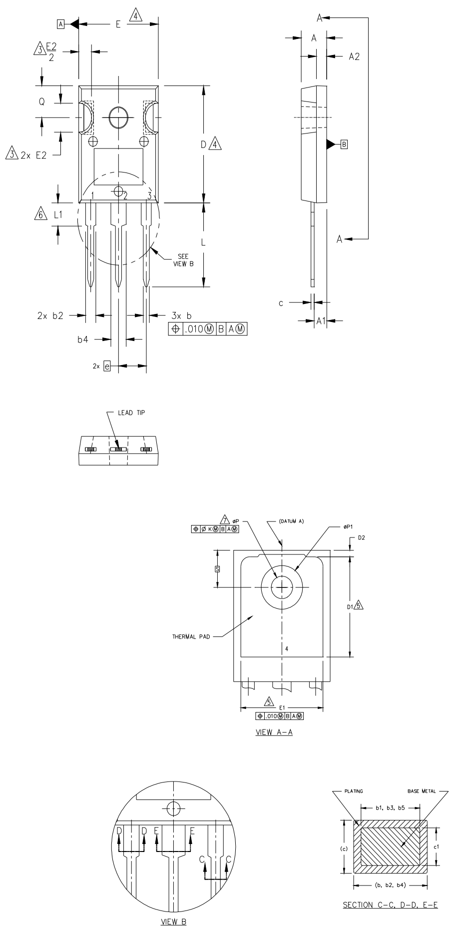


Figure 25b Gate Charge Waveform

5 Package Information

TO-247AC Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

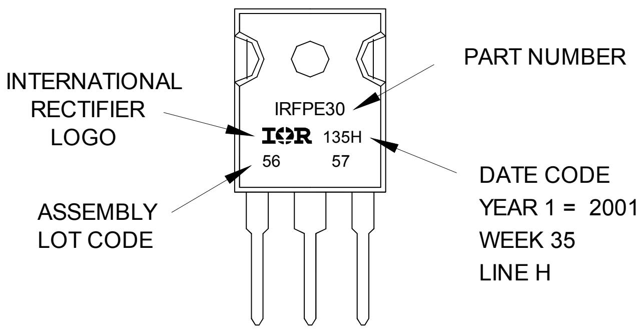
DIODES

1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

6 Qualification Information

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	1.0	2017-03-16	• First release data sheet.

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