# Si5315-EVB User's Guide

## Description

The Si5315 Evaluation Board User's Guide provides for a complete and simple evaluation of the functions, features, and performance of the Si5315-EVB.

The Si5315 Synchronous Ethernet/Telecom jitter attenuating clock multiplier has a comprehensive feature set, including any-rate frequency synthesis, multiple clock inputs, multiple clock outputs, alarm and status outputs, hitless switching between input clocks, and programmable output clock signal format (LVPECL, LVDS, CML, CMOS). For more details, consult the Silicon Labs timing products website at: www.silabs.com/timing.

TheSi5315-EVB has two differential clock input and output ports that are AC terminated to 50 ohms and then AC coupled to the Si5315. The XA-XB reference is usually a 40 MHz crystal; however, there are provisions for an external XA-XB reference clock (either differential or single ended).

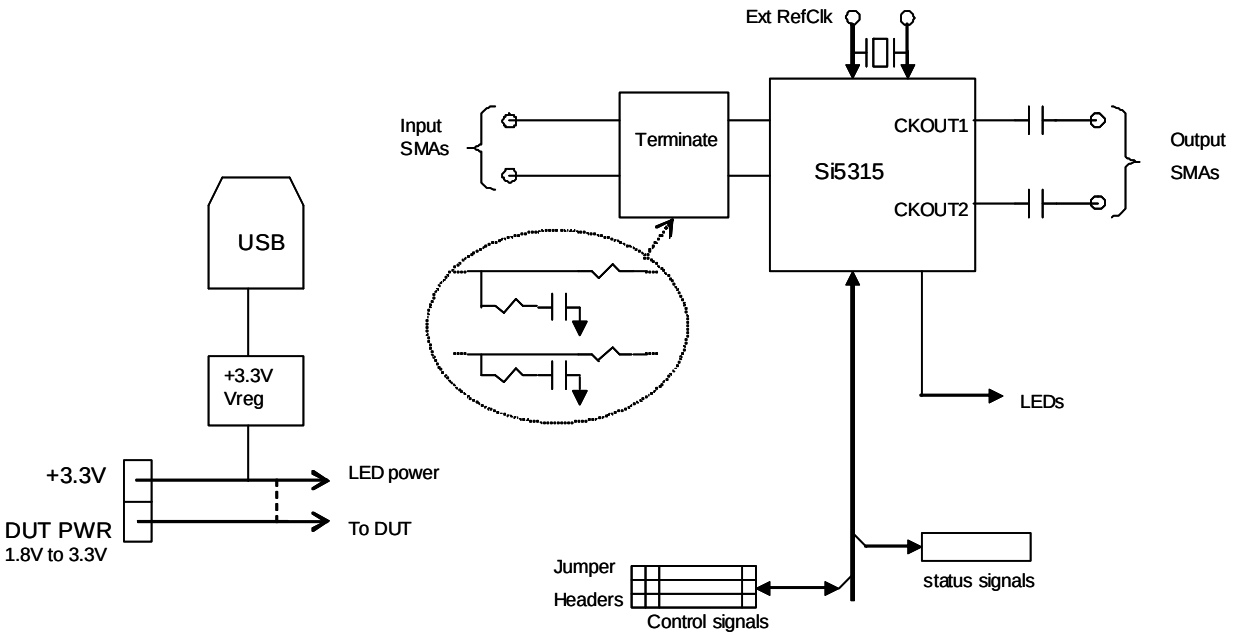
The evaluation board (EVB) can be powered using two different approaches: external power supplies or by USB. Jumper plugs are provided to select between these two options. Jumper plugs are used to strap the device pins for the various pin value options. Status outputs are available on a ribbon connector header. SMA connectors are used for the clock input, output, and XA-XB reference signals.

## Features

The Si5315-EVB includes the following:

- CD with the Si5315 documentation and the Si5315-EVB User's Guide
- Evaluation board

## Function Block Diagram





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## 1. Introduction

The Si5315 is a jitter-attenuating clock multiplier for Gb and 10G Synchronous Ethernet, SONET/SDH, and PDH (T1/E1) applications. The Si5315 accepts dual clock inputs ranging from 8 kHz to 644.53 MHz and generates two equal frequency-multiplied clock outputs ranging from 8 kHz to 644.53 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SyncE and T1/E1 rates. The Si5315 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is user programmable, providing jitter performance optimization at the application level.

Refer to the Si5315 data sheet for technical details of the device.

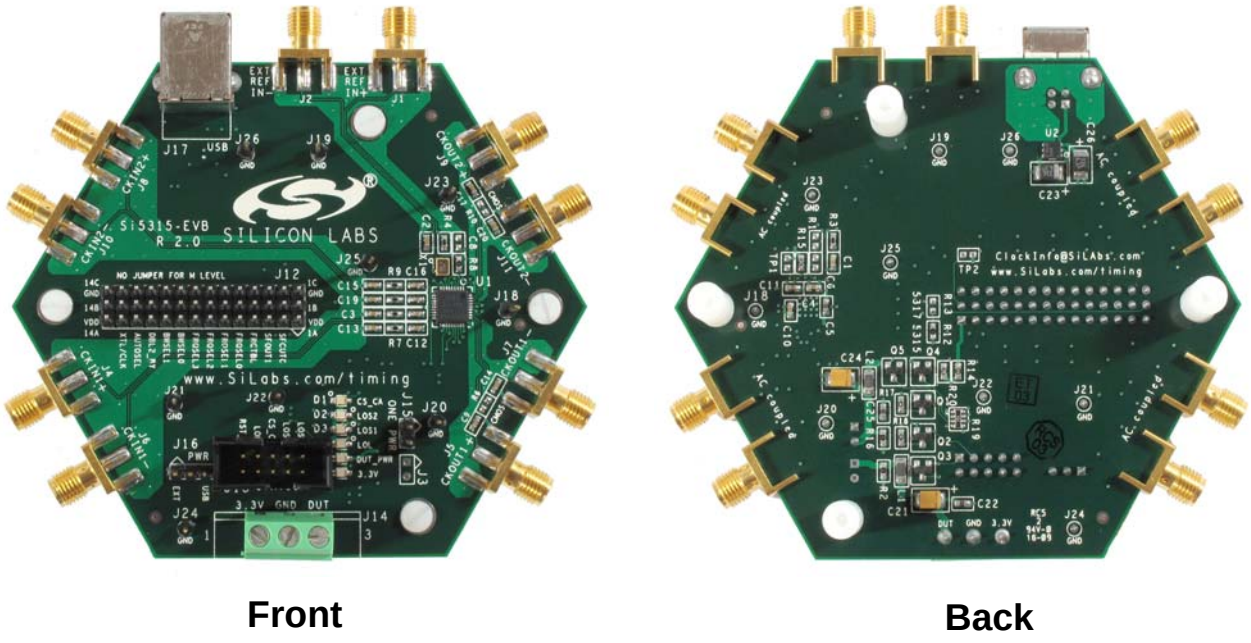


**Figure 1. Si5315 EVB**

# 2. Si53315-EVB Input and Output Clocks

Refer to the schematics, diagrams, and tables while reading this section.

## 2.1. Input Clocks

The Si5315 has two differential clock inputs that are AC terminated and AC coupled before being presented to the Si5315. If the input clock frequencies are low (below 1 MHz), there are extra considerations that should be taken into account. The Si5315 has a maximum clock input rise time specification of 11 ns that must be met (see CKNtrf in the Si5315 data sheet). Also, if the input clock is LVCMOS, it might be advantageous to replace the input coupling capacitors (C7, C12, C16, and C18) with zero ohm resistors. Regardless of the input format, if the clock inputs are not roughly 50% duty cycle, it is highly recommended to avoid AC coupling. For input clocks that are far off of 50% duty cycle, the average value of the signal that passes through the coupling capacitor will be significantly off of the midpoint between the maximum and minimum value of the clock signal, resulting in a mismatch with the common mode input threshold voltage (see $V_{ICM}$ in Table 2 of the Si5315 data sheet).

## 2.2. XA-XB Reference

To achieve very low jitter generation and for stability during holdover, the Si5315 requires a stable, low jitter reference at its XA-XB pins. To that end, the EVB is configured with a 40 MHz fundamental mode crystal connected between pins 6 and 7 of the Si5315. However, the Si5315-EVB is capable of using an external XA-XB reference oscillator, either differential or single ended. J1 and J2 are the SMA connectors with AC termination. AC coupling is also provided that needs to be installed at C6 and C8. Table 1 explains the changes of components that are needed to implement an external XA-XB reference oscillator.

**Table 1. XA-XB Reference Mode of Operation**

| | **Mode** | |
|---|---|---|
| | **Xtal** | **Ext Ref** |
| Ext Ref In+ | NC | J1 |
| Ext Ref In- | NC | J2 |
| C6, C8 | NOPOP | install |
| R8 | install | NOPOP |
| XTAL/CLOCK (J12 jumper, see Table 3.) | L | M |

**Notes:**
1. Xtal is 40 MHz.
2. NC – no connect.
3. NOPOP – do not install.

## 2.3. Output Clocks

The clock outputs are AC coupled and are available on SMA's J5, J7, J9, and J11. For LVCMOS outputs, it might be desirable to replace the AC coupling capacitors (C9, C14, C17, and C 20) with zero ohm resistors. Also, if greater drive strength is desired for LVCMOS outputs, R6 and R10 can be installed.

## 2.4. Pin Configuration

J12 is the large jumper header in the center left of the board that implements the jumper plugs that configure the pins of the Si5315. Each pin can be strapped to be either H, M or L. H is achieved by installing a jumper plug between the appropriate middle row pin and its VDD row pin. L is achieved by installing a jumper plug between the appropriate middle row pin and its GND row pin. M is achieved by not installing a jumper plug.

## 2.5. Evaluation Board Power Options

The EVB can be powered from two possible sources: USB or external supplies. A 3.3 V supply is required to run the LEDs because of their large forward drop. The Si5315 power supply can be separated from the 3.3 V supply so that the Si5315 can be evaluated at voltages other than 3.3 V. It is important to note that when the USB supply is being used, the EVB uses the USB port only for power and that the resulting power supply is strictly 3.3 V.

Here are the instructions for the various possibilities:

### 2.5.1. Two External Power Supplies

1. Install a jumper between J16.1 and J16.2 (labeled EXT).
2. No USB connection.
3. If the Si5315 is not being operated at 3.3 V, two different supplies should be connected to J14. Connect the 3.3 V supply to J14.1 and J14.2 (labeled 3.3 V and GND). Connect the SI5315 power supply between J14.2 and J14.3 (labeled GND and DUT).
4. If the Si5315 is to be operated at 3.3 V, J15 (labeled ONE PWR) can be installed, requiring only one external supply. Connect 3.3 V power between J14.2 and J14.3 (labeled GND and DUT).

### 2.5.2. USB Power

1. With a USB cable, plug the EVB into a powered USB port.
2. Install a jumper between J16.2 and J16.3 (labeled USB).
3. Install a jumper at J15 (labeled ONE PWR).

### 2.5.3. USB 3.3 V Power, External Si5315 Power

1. Install a jumper between J16.2 and J16.3 (labeled USB).
2. No jumper at J15 (labeled ONE PWR).
3. Connect the Si5315 power supply between J14.2 and J14.3 (labeled GND and DUT).

# 3. Connectors and LEDs

## 3.1. LEDs

**Table 2. LED Descriptions**

| LED | Color | Label | Significance |
|---|---|---|---|
| D1 | Yellow | CS_CA | ON = clock input 2 selected, else clock 1 |
| D2 | Red | LOS2 | ON = no valid clock input 2 |
| D3 | Red | LOS1 | ON = no valid clock input 1 |
| D4 | Red | LOL | ON = Si5315 is not locked |
| D5 | Green | DUT_PWR | ON = Si5315 power is present |
| D6 | Green | 3.3V | ON = 3.3V power is present |

## 3.2. Connectors, Headers, and Jumpers

Refer to Figure 2 to locate the items described in this section.

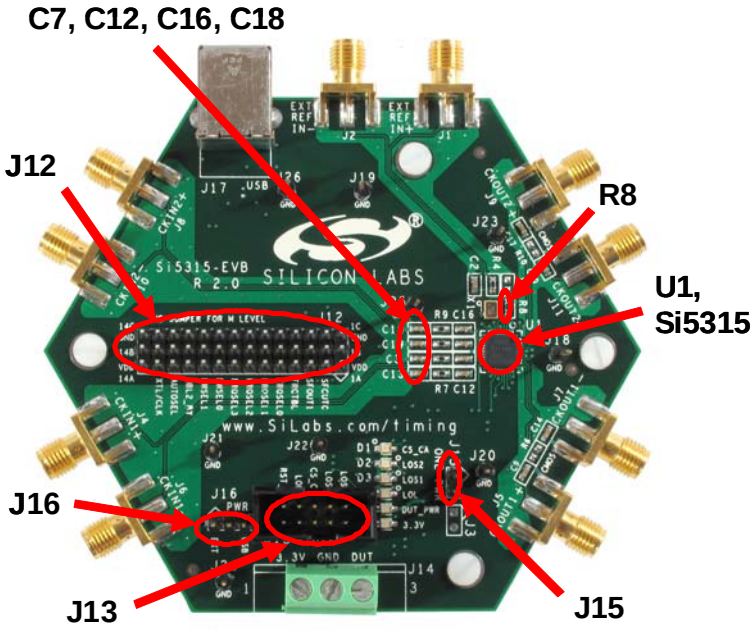


**Figure 2. Connectors, Headers, and Jumper Locations**

**Table 3. Configuration Header, J12**

| J12 | Pin |
|---|---|
| J12.1 | Not used* |
| J12.2 | SFOUT0 |
| J12.3 | SFOUT1 |
| J12.4 | FRQTBL |
| J12.5 | FRQSEL0 |
| J12.6 | FRQSEL1 |
| J12.7 | FRQSEL2 |
| J12.8 | FRQSEL3 |
| J12.9 | BWSEL0 |
| J12.10 | BSWEL1 |
| J12.11 | DBL2_BY |
| J12.12 | AUTOSEL |
| J12.13 | XTAL/CLOCK |
| J12.14 | Not used* |
| ***Note:** Unused header pin locations should be left open. | |

**Table 4. Status Indication Header, J13**

| J13 | Signal |
|---|---|
| J13.1 | LOS1 |
| J13.3 | LOS2 |
| J13.5 | CS_CA |
| J13.7 | LOL |
| J13.9 | RST_B |

# 4. Schematics

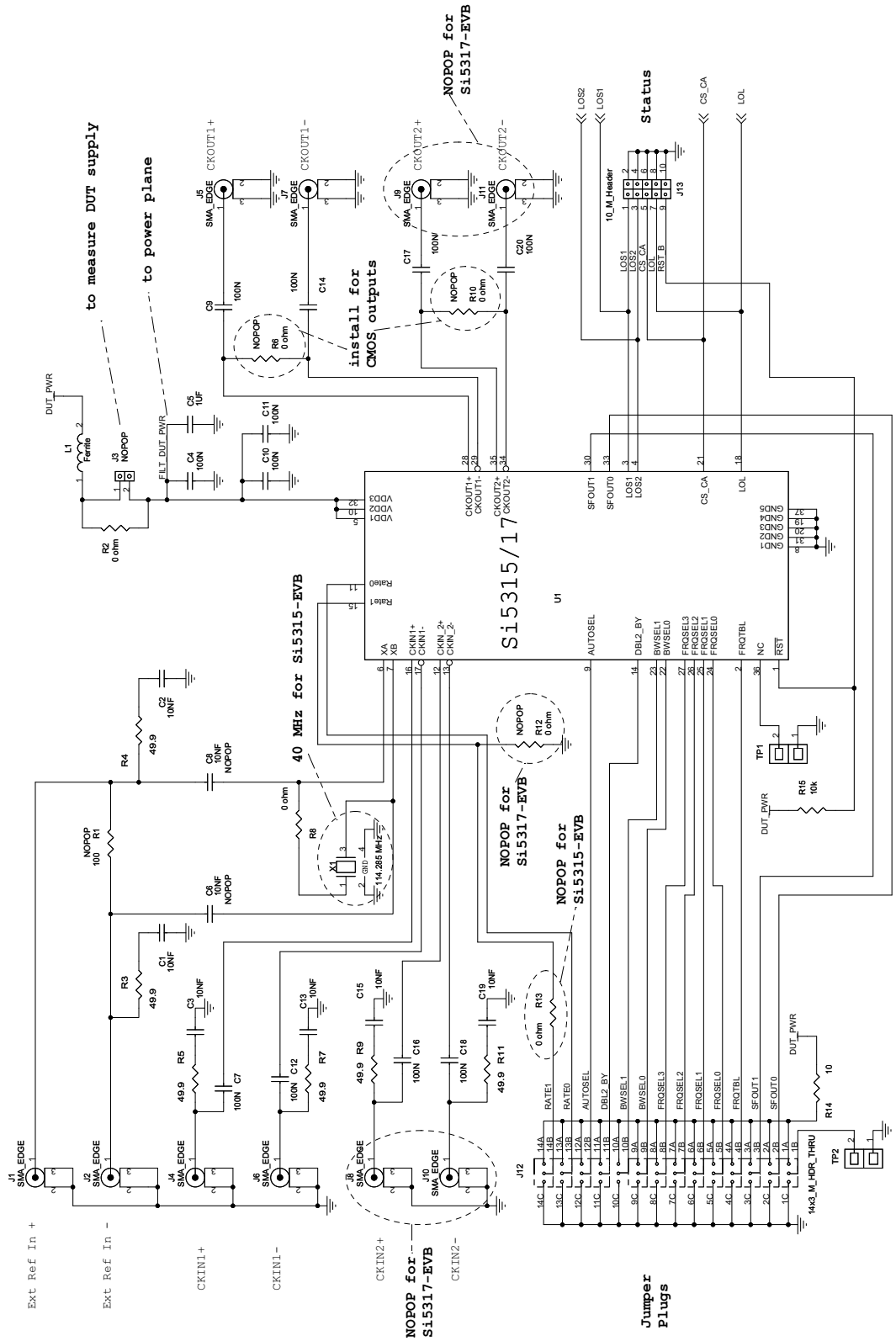


Figure 3. Si5315/17-EVB

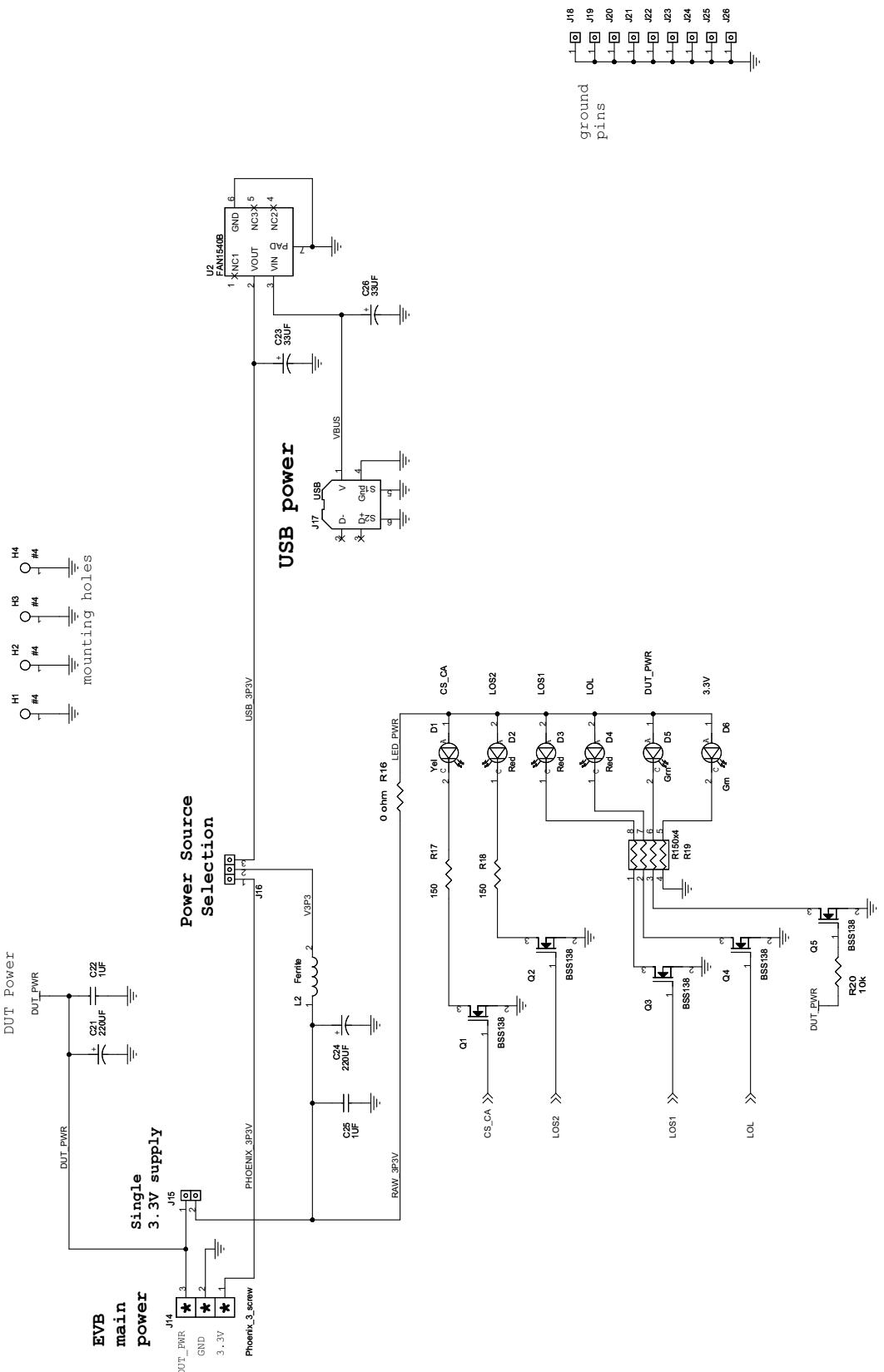


**Figure 4. Power and LED**

## 5. Bill of Materials

**Table 5. Si5315-EVB Bill of Materials**

| Item | Qty | Reference | Part | Mfr | Manufacturer Part No. |
|---|---|---|---|---|---|
| 1 | 6 | C1,C2,C3,C13,C15,C19 | 10NF | Venkel | C0603X7R160-103KNE |
| 2 | 11 | C4,C7,C9,C10,C11,C12,C14, C16,C17,C18,C20 | 100N | Venkel | C0603X7R160-104KNE |
| 3 | 3 | C5,C22,C25 | 1UF | Venkel | C0603X7R6R3-105KNE |
| 5 | 2 | C21,C24 | 220UF | Kemet | T494B227M004AT |
| 6 | 2 | C23,C26 | 33UF | Venkel | TA006TCM336MBR |
| 7 | 1 | D1 | Yel | Panasonic | LN1471YTR |
| 8 | 3 | D2,D3,D4 | Red | Lumex | LN1271RAL |
| 9 | 2 | D5,D6 | Grn | Panasonic | LN1371G |
| 11 | 10 | J1,J2,J4,J5,J6,J7, J8,J9,J10,J11 | SMA_EDGE | Johnson | 142-0701-801 |
| 13 | 1 | J12 | 14x3_M_HDR_THRU | — | |
| 14 | 1 | J13 | 10_M_Header | 3M | N2510-6002RB |
| 15 | 1 | J14 | Phoenix_3_screw | Phoenix | MKDSN 1.5/3-5.08 |
| 16 | 1 | J15 | Jmpr_2pin | | |
| 17 | 1 | J16 | Jmpr_3pin | | |
| 18 | 1 | J17 | USB | FCI | 61729-0010BLF |
| 19 | 9 | J18,J19,J20,J21, J22,J23,J24,J25,J26 | Jmpr_1pin | | |
| 20 | 2 | L1,L2 | Ferrite | Venkel | FBC1206-471H |
| 21 | 5 | Q1,Q2,Q3,Q4,Q5 | BSS138 | On Semi | BSS138LT1G |
| 23 | 4 | R2,R8,R12,R16 | 0 ohm | Venkel | CR0603-16W-000T |
| 24 | 6 | R3,R4,R5,R7,R9,R11 | 49.9 | Venkel | CR0603-16W-49R9FT |
| 26 | 1 | R14 | 10 | Venkel | CR0603-16W-10R0FT |
| 27 | 2 | R15,R20 | 10k | Venkel | CR603-16W-1002FT |
| 28 | 2 | R17,R18 | 150 | Venkel | CR0603-16W-1500FT |
| 29 | 1 | R19 | R150x4 | Panasonic | EXB-38V151JV |
| 31 | 1 | U1 | Si5315 | Silicon Labs | Si5315A-C-GM |

**Table 5. Si5315-EVB Bill of Materials**

| Item | Qty | Reference | Part | Mfr | Manufacturer Part No. |
|---|---|---|---|---|---|
| 32 | 1 | U2 | FAN1540B | Fairchild | FAN1540BPMX |
| 33 | 1 | X1 | 40 MHz | Abracon | ABM8-40.000 MHz-BZT |
| **Not Populated** | | | | | |
| 4 | 2 | C6,C8 | 10NF | Venkel | C0603X7R160-103KNE |
| 12 | 1 | J3 | Jmpr_2pin | | |
| 22 | 1 | R1 | 100 | Venkel | CR0603-16W-1000FT |
| 25 | 3 | R6,R10,R13 | 0 ohm | Venkel | CR0603-16W-000T |

## 6. Layout

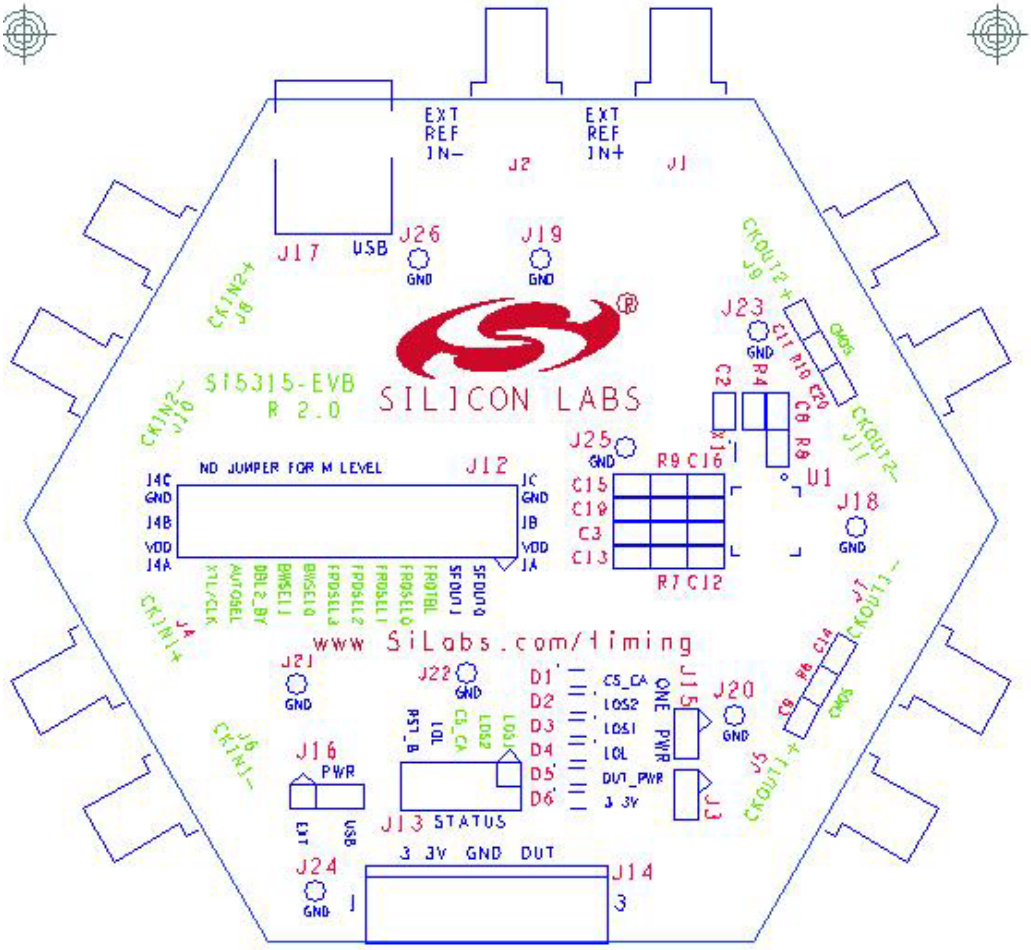


**Figure 5. Silkscreen Top**

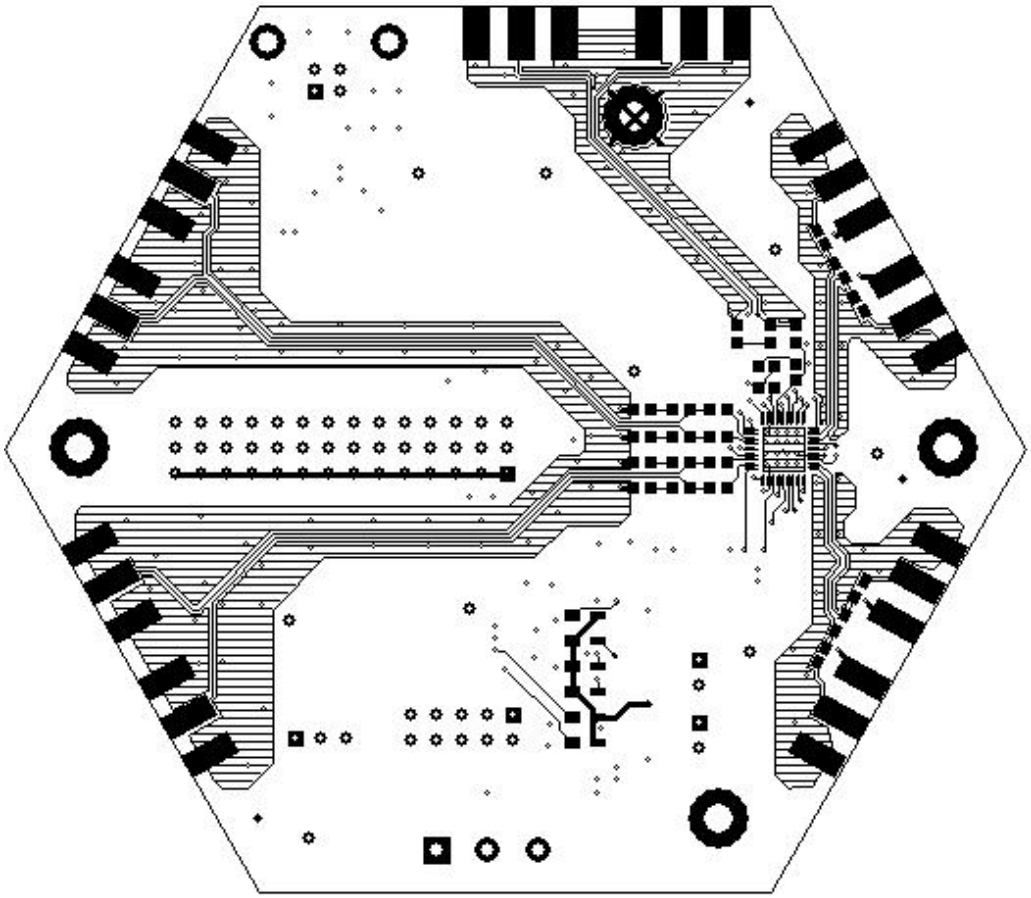

**Figure 6. Layer 1**

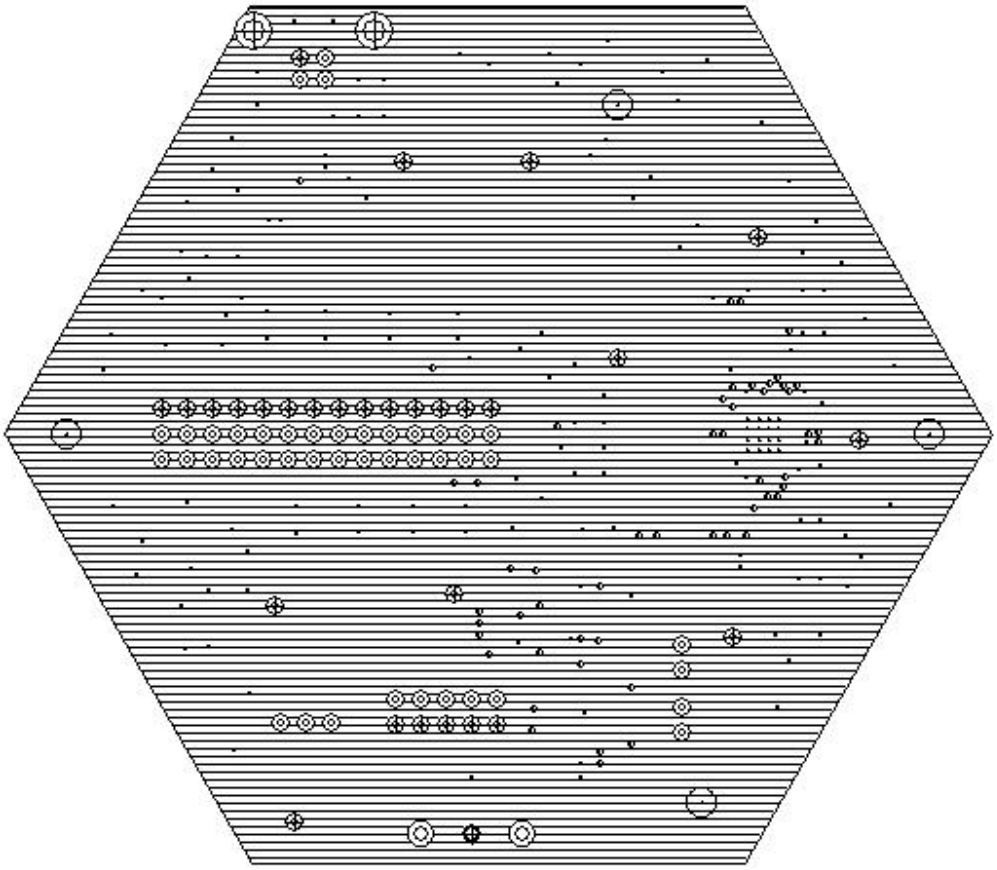

**Figure 7. Layer 2—Ground Plane**

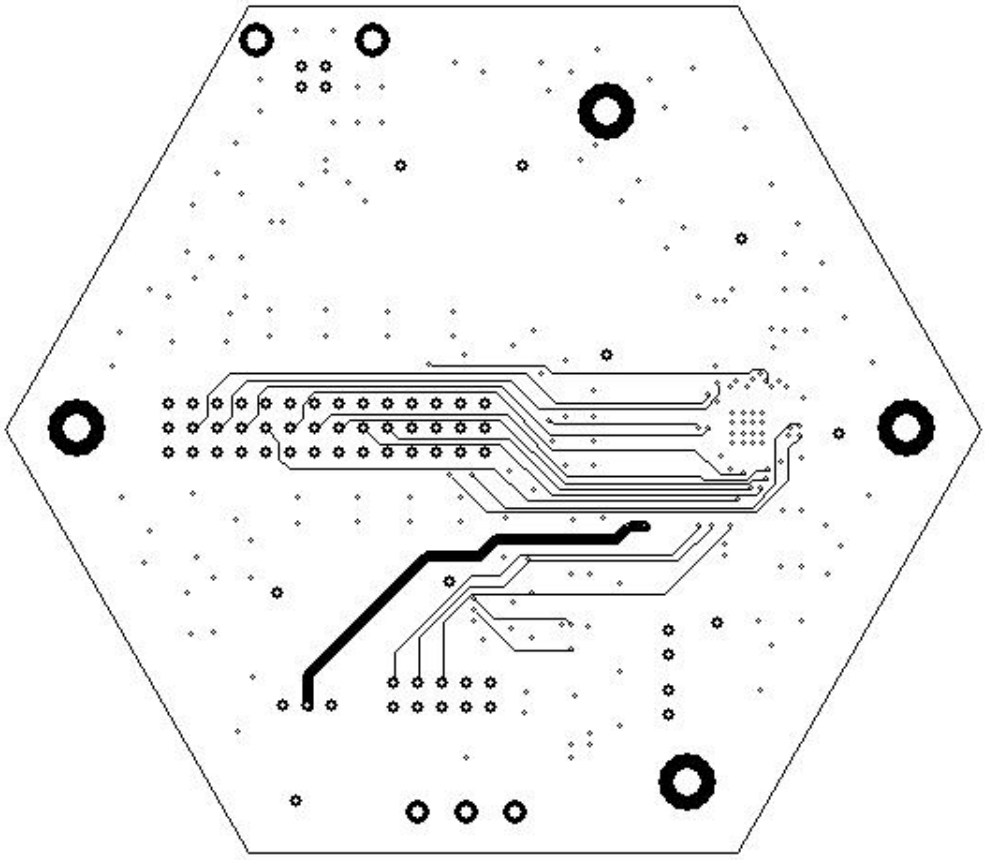

**Figure 8. Layer 3**

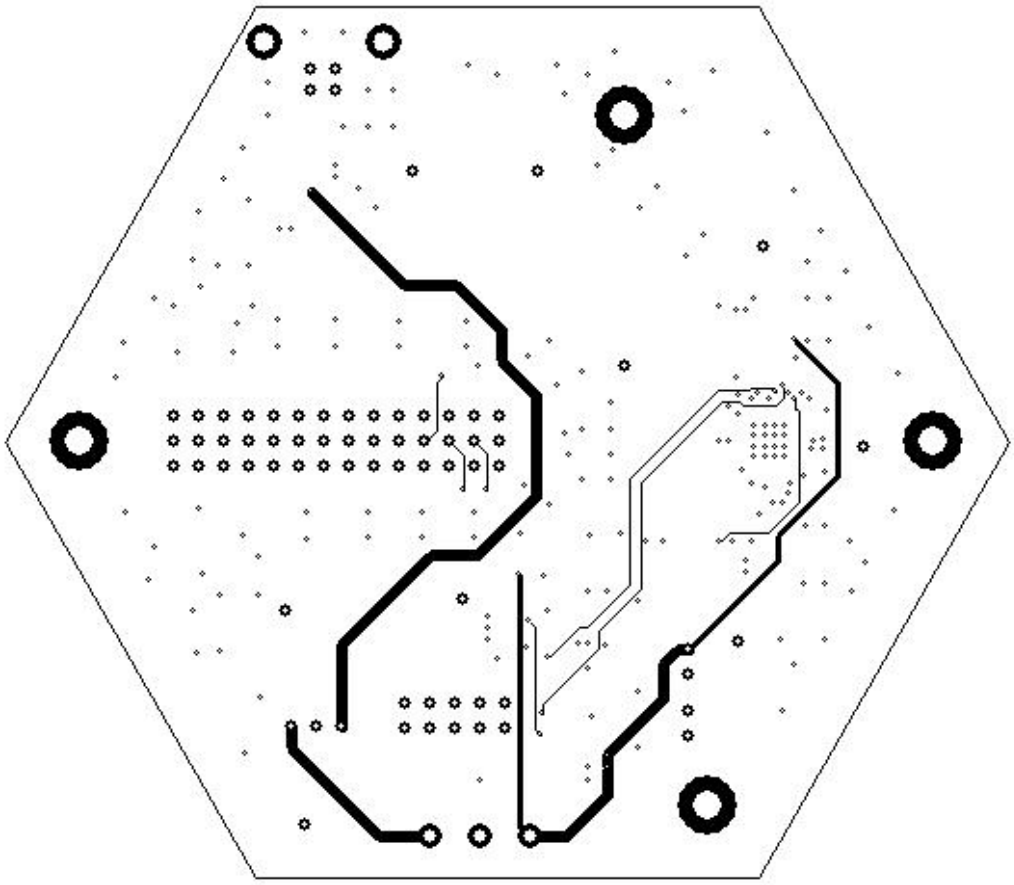

**Figure 9. Layer 4**

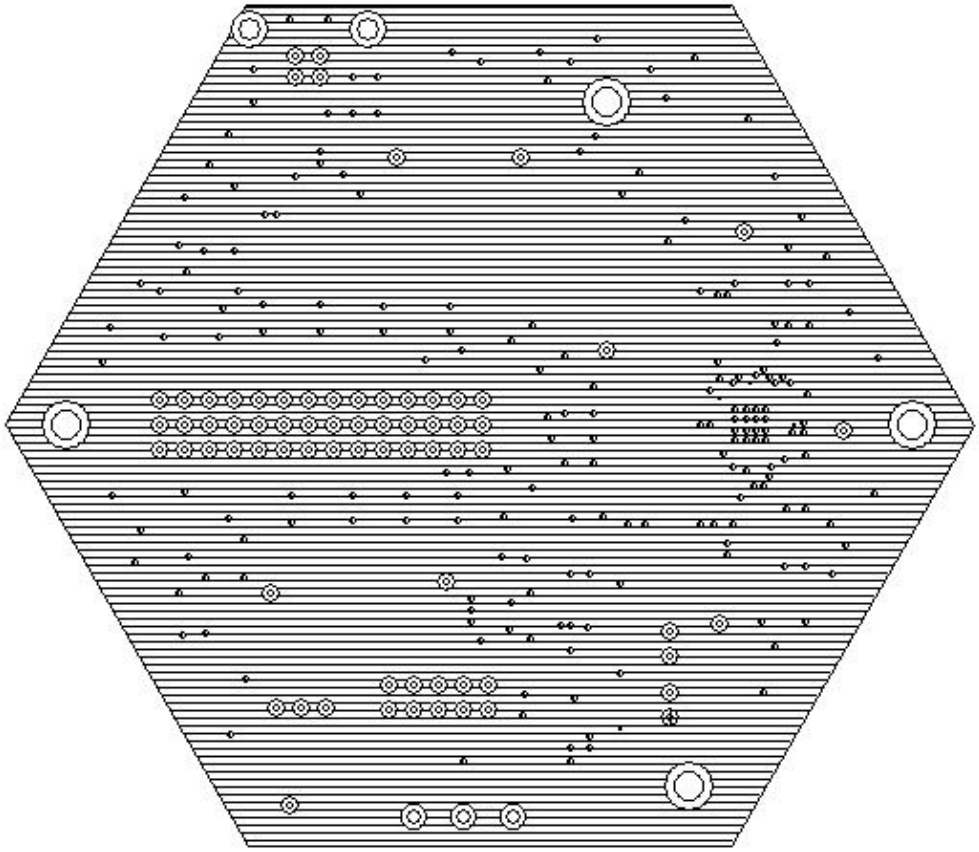

**Figure 10. Layer 5, FILT_DUT_PWR**

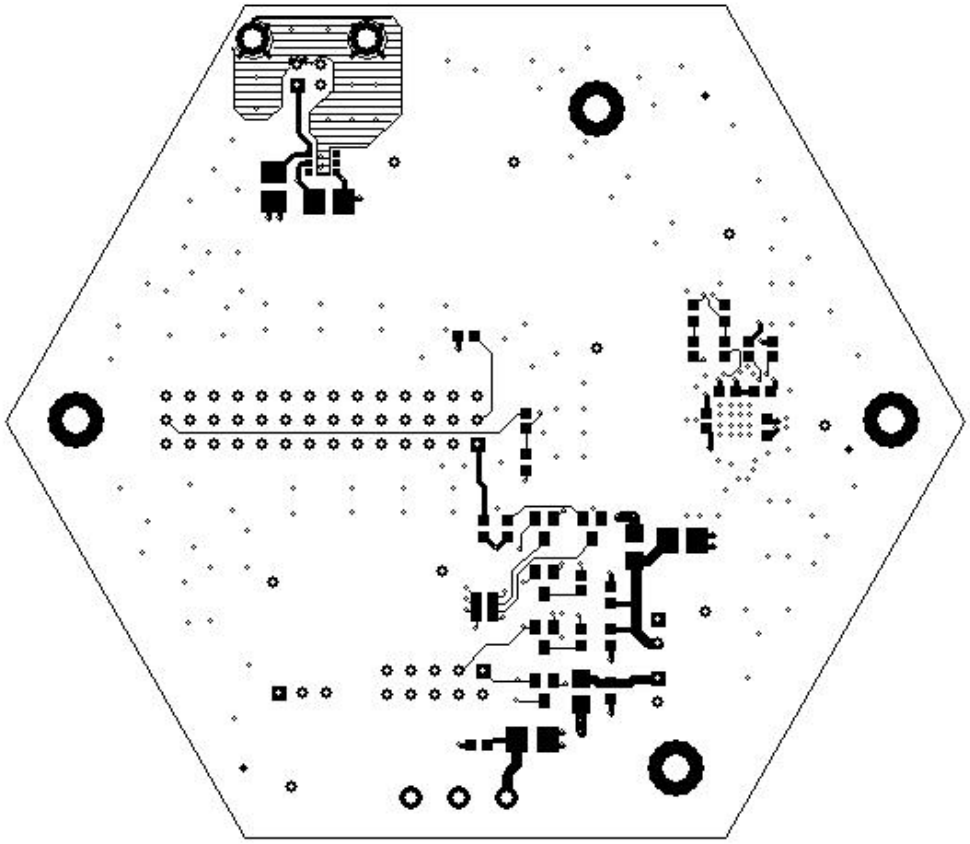

**Figure 11. Layer 6, Bottom**

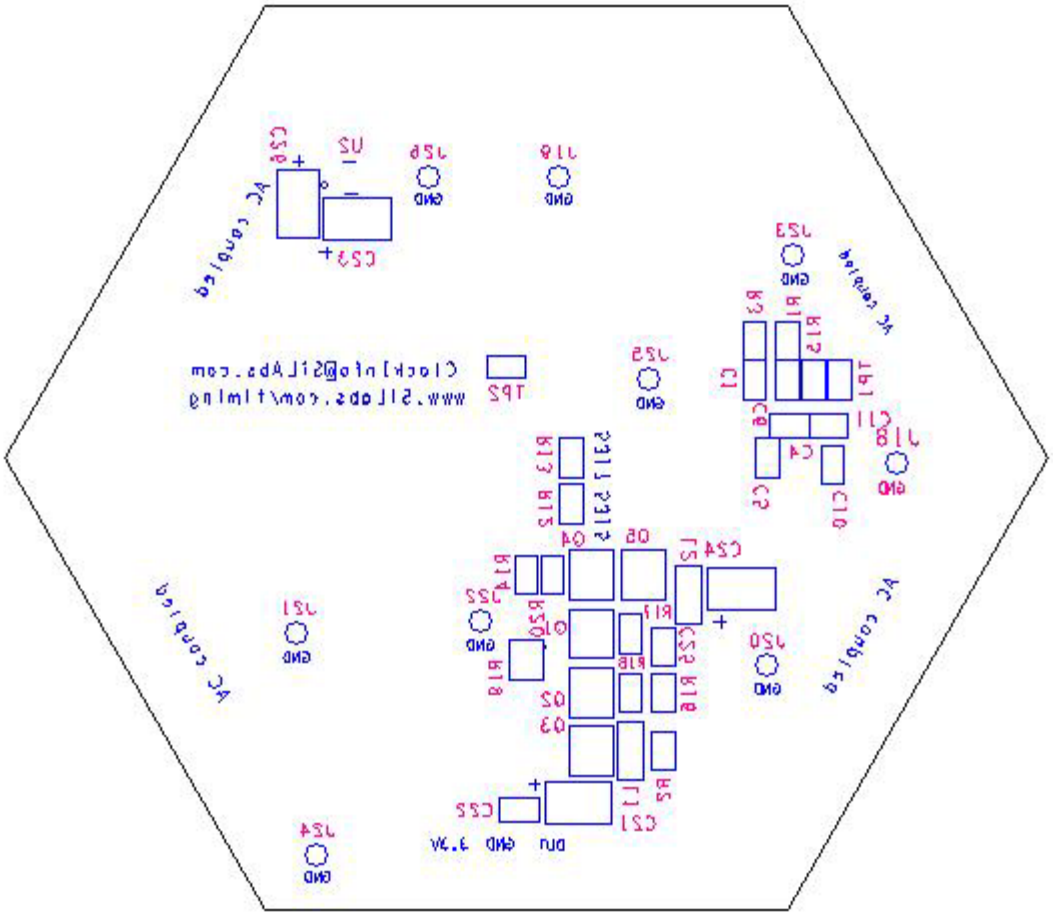

**Figure 12. Bottom Silkscreen**

# 7. Factory Default Configuration

**Table 6. Factory Default Jumper Settings**

| J12 | Pin | Jumper |
|---|---|---|
| J12.1 | Not used | — |
| J12.2 | SFOUT0 | H |
| J12.3 | SFOUT1 | M |
| J12.4 | FRQTBL | H |
| J12.5 | FRQSEL0 | L |
| J12.6 | FRQSEL1 | H |
| J12.7 | FRQSEL2 | M |
| J12.8 | FRQSEL3 | L |
| J12.9 | BWSEL0 | H |
| J12.10 | BSWEL1 | H |
| J12.11 | DBL2_BY | L |
| J12.12 | AUTOSEL | H |
| J12.13 | XTAL/CLOCK | L |
| J12.14 | Not used | — |

The jumper settings in Table 6 result in the following:
SFOUT = LVPECL outputs
19.44 MHz input clocks
155.52 MHz output clocks
BW = 112 Hz
DBL2_BY = CKOUT2 enabled
AUTOSEL = automatic revertive clock selection
XTAL/CLOCK = 40 MHz crystal
Refer to Table 7 in the Si5315 Data Sheet for other frequency plans.

The factory configuration for the board is to use only USB power by using the following jumper configuration:

Jumper between J16.2 and J16.3 (labeled PWR, USB)
Jumper installed on J15 (labeled ONE POWER)

## NOTES:

# DOCUMENT CHANGE LIST

## Revision 0.1 to Revision 0.2

- Removed Si5315-EVB from Appendix of Si5315-EVB, Si5316-EVB, Si5319-EVB, Si532/23-EVB, Si5325/26-EVB with Si5315-EVB Appendix B User's Guide
- Revised Revision 0.2 as a stand-alone Si5315-EVB User's Guide


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